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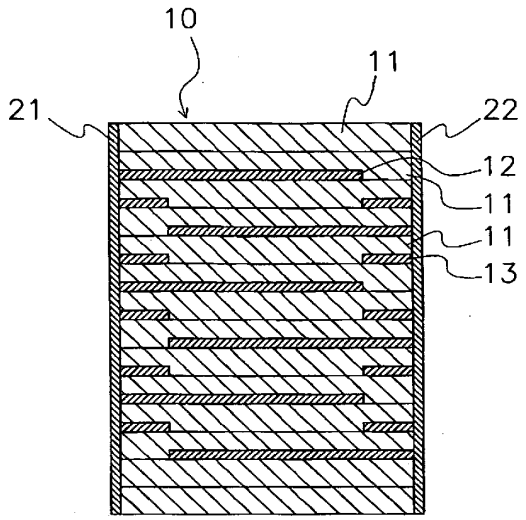
(54) MULTILAYER PIEZOELECTRIC DEVICE

(57) To provide a monolithic piezoelectric element that can be easily manufactured while the stack is prevented from being mechanically broken by stress.

The monolithic piezoelectric element includes a stack 10, and the stack 10 includes a crack-forming conductive layer 13 for forming a small crack therein. The small crack alleviates stress, thereby preventing the occurrence of such a large crack as extends to the piezoelectrically active region.

FIG. 1



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Description

Technical Field

[0001] The present invention relates to monolithic piezoelectric elements, such as monolithic piezoelectric actuators.

Background Art

[0002] Monolithic piezoelectric elements are known as a type of piezoelectric element that converts electric energy into mechanical energy using an electrostrictive effect of solid material. The monolithic piezoelectric element is formed by alternately stacking piezoelectric ceramic layers and internal conductive layers.

[0003] The monolithic piezoelectric element has a similar structure as monolithic ceramic capacitors, and the internal conductive layers are alternately connected to one and the other external electrode. When a voltage is applied to the two external electrodes, an electric field is generated between each of the two adjacent internal conductors, and thus, distortion occurs in the ceramic layers.

[0004] However, the electric field is generated to cause distortion only in a region (piezoelectrically active region) where the internal conductive layers overlap when viewed in the stacking direction, and the distortion does not occur in the other region (piezoelectrically inactive region), where the internal conductors do not overlap and hence no electric field is generated.

[0005] Consequently, when a large distortion is produced by applying a voltage, a high stress is generated at the boundary between the piezoelectrically active region and the piezoelectrically inactive region. The stress may mechanically break the stack. For example, a large crack may occur between the internal conductive layer and the ceramic layer.

[0006] In order to prevent the stack from being broken by the internal stress, Patent Document 1 has disclosed that a grooves extending in a direction parallel to the internal conductive layers are formed in a side surface parallel to the stacking direction of the stack. Hence, the invention of Patent Document 1 alleviates the concentration of the stress by removing part of the piezoelectrically inactive region.

[0007] Patent Document 1: Japanese Examined Patent Application Publication No. 6-5794

Disclosure of Invention

Problems to be Solved by the Invention

[0008] Although Patent Document 1 does not disclose the process for forming the grooves in detail, they may be formed by, for example, using ceramic green sheets on which a vanishing material such as carbon paste has been printed. The vanishing material is eliminated during firing, thus forming the grooves. The grooves may be cut in the stack with a wire saw after firing.

[0009] However, these methods have disadvantages.

[0010] In the method of eliminating the vanishing material to form the grooves, the piezoelectric ceramic layers are fused and bonded together after disappearance of the vanishing material because the vanishing material disappears at a temperature lower than the firing temperature of the piezoelectric ceramic layers. Consequently, the grooves cannot be formed in a desired shape.

[0011] The method using a wire saw is inferior in processing precision, and it cannot be applied to the process using thin ceramic layers. In addition, the processing cost is high, and accordingly the manufacturing cost is increased.

[0012] Accordingly, an object of the present invention is to provide a monolithic piezoelectric element that can be easily manufactured while the stack is prevented from being mechanically broken by stress.

Means for Solving the Problems

[0013] In order to overcome the above-mentioned problems, a monolithic piezoelectric element according to the present invention includes a stack including piezoelectric ceramic layers and internal conductive layers that are integrally formed, and external electrodes formed on the surface of the stack. The stack further includes a crack-forming conductive layer arranged inside the stack so as to form a crack in the stack.

[0014] By forming the crack-forming conductive layer, a tiny crack can be intentionally formed in the vicinity of the crack-forming conductive layer, and thus stress can be reduced. Thus, the occurrence of a large crack that degrades the performance of the element can be prevented.

[0015] In the monolithic piezoelectric element according to the present invention, the interfacial strength between the crack-forming conductive layer and the ceramic layer may be lower than the interfacial strength between the internal conductive layer and the ceramic layer.

[0016] Thus, a tiny crack can be preferentially formed at the interface between the crack-forming conductive layer and the ceramic layer having a lower interfacial strength. The tiny crack can effectively prevent a large crack that degrades the performance of the element.

[0017] The technique for reducing the interfacial strength between the crack-forming conductive layer and the ceramic layer to lower than the interfacial strength between the internal conductive layer and the ceramic layer is not particularly limited. For example, it can be realized in a structure in which the internal conductive layers contain a ceramics having the same composition system as the ceramic contained in the ceramic layers, and in which the crack-forming conductive layer does not contain the ceramics having the same composition system as the ceramic of the ceramic layer or contains an amount of the ceramics that is a lower than the amount of the internal conductive layer.

[0018] By adding to a conductor a ceramics having the same composition system as the ceramic contained in the ceramic layer, the interfacial strength between the conductor and the ceramic layer is increased. Accordingly, the interfacial strength between the crack-forming conductive layer and the ceramic layer can be reduced to lower than the interfacial strength between the internal conductive layer and the ceramic layer by adding the ceramic to the internal conductive layer to enhance the interfacial strength between the internal conductive layer and the ceramic layer while the crack-forming conductive layer contains the ceramic in a lower proportion or does not contain the ceramic.

[0019] Ceramics having the same composition systems each other refer to ceramics containing the same element as a principal constituent. Preferably, the internal conductive layer contains a ceramic having the same composition as the ceramic contained in the ceramic layers.

[0020] The crack-forming conductive layer may have a larger thickness than the internal conductive layer.

[0021] As the thickness of a conductor is reduced, ceramic cross-links are more easily formed in the conductor, and accordingly the interfacial strength between the conductor and the ceramic layer is increased. Therefore, the interfacial strength between the crack-forming conductive layer and the ceramic layer can be reduced to lower than the interfacial strength between the internal conductive layer and the ceramic layer by increasing the thickness of the crack-forming conductive layer so as to be greater than the thickness of the internal conductive layer.

[0022] In the monolithic piezoelectric element according to the present invention, the crack-forming conductive layer is preferably disposed along a surface of the layers of the stack, and may be disposed on the same surfaces as the internal conductive layers or on surfaces on which the internal conductive layers are not formed.

[0023] Preferably, the crack-forming conductive layer is arranged to avoid the region where the internal conductive layers overlap in a direction in which the layers are stacked, that is, the piezoelectrically active region. Thus, the internal stress produced at the boundary between the piezoelectrically active region and the piezoelectrically inactive region can be eliminated, and cracks can be prevented from extending to the piezoelectrically active region. Consequently, the degradation of the performance of the monolithic piezoelectric element can be prevented.

[0024] In the monolithic piezoelectric element according to the present invention, when sections are defined by dividing the stack by the surfaces of layers on which the crack-forming conductive layer is disposed, the number of sections is M, and the distortion in the stacking direction is D (μm), the distortion per section D/M may be 7.5 μm or less.

[0025] Thus, a large crack that leads to degradation of the performance of the element can be prevented from occurring effectively.

Advantages

[0026] According to the present invention, the presence of the crack-forming conductive layer intentionally forms a tiny crack to alleviate stress, and consequently prevents the occurrence of large cracks and thus the degradation of the element performance. In addition, since it is not necessary to use a vanishing material or to form a groove with a wire saw, the element can be easily manufactured by a known stacking process.

Brief Description of the Drawings

[0027]

Fig. 1 is a sectional view of a monolithic piezoelectric element according to a first embodiment of the present invention.

Fig. 2 is a fragmentary sectional view of the monolithic piezoelectric element according to the first embodiment of the present invention.

Fig. 3 is a perspective view of a process for manufacturing the monolithic piezoelectric element according to the first embodiment of the present invention.

Fig. 4 is a perspective view of a modification of the monolithic piezoelectric element according to the present invention.

Fig. 5 is a sectional view of a monolithic piezoelectric element according to a second embodiment of the present invention.

Fig. 6 is a perspective view of a process for manufacturing the monolithic piezoelectric element according to the

second embodiment of the present invention.

Fig. 7 is a perspective view of a modification of the monolithic piezoelectric element according to the present invention.

Reference Numerals

[0028]

10: stack
11: ceramic layer
12: internal conductive layer
13: crack-forming conductive layer
21, 22: external electrode

Best Mode for Carrying Out the Invention

[0029] The best mode for carrying out the present invention will now be described with reference to the drawings.

Embodiment 1

[0030] Fig. 1 is a sectional view of a monolithic piezoelectric element according to a first embodiment of the invention. The monolithic piezoelectric element includes a stack 10 and external electrodes 21 and 22 disposed on surfaces of the stack 10. The stack 10 includes integrally formed ceramic layers 11, internal conductive layers 12 and crack-forming conductive layers 13.

[0031] The ceramic layers 11 are made of a piezoelectric ceramics, such as lead zirconate titanate (PZT).

[0032] The internal conductive layers 12 mainly contain a metal, such as Ag or Pd, and are alternately connected to one and the other external electrodes 21 and 22, respectively.

[0033] The crack-forming conductive layers 13 mainly contain a metal, such as Ag or Pd, and are disposed in regions (piezoelectrically inactive regions) where the internal conductive layers 12 do not overlap in the stacking direction. The crack-forming conductive layers 13 are disposed on the surfaces of the ceramic layers not having the internal conductive layers 12. Although Fig. 1 shows the internal conductive layers 12 have substantially the same thickness as the crack-forming conductive layers 13, the crack-forming conductive layers 13 have a larger thickness than the internal conductive layers 12.

[0034] The external electrodes 21 and 22 mainly contain a metal, such as Ag, and formed on surfaces of the stack 10.

[0035] Fig. 2 is a fragmentary enlarged sectional view schematically showing the crack-forming conductive layer 13 and its vicinity. A tiny crack 14 is formed at the interface between the crack-forming conductive layer 13 and the ceramic layer 11 after polarization. This crack 14 does not extend to the piezoelectrically active region defined by overlapping the internal conductive layers 12. There is no crack at the interface between the internal conductive layer 12 and the ceramic layer 11. This is because the presence of the crack-forming conductive layer 13 intentionally forms a tiny crack 14 at the interface between the crack-forming conductive layer 13 and the ceramic layer 11, thereby reducing the stress.

[0036] A method for manufacturing the monolithic piezoelectric element will now be described with reference to Fig. 3.

[0037] First, predetermined weights of metal oxides, such as titanium oxide, zirconium oxide, and lead oxide, are weighed out, and the mixture is calcined to yield a piezoelectric PZT ceramics. The piezoelectric ceramics is pulverized into piezoelectric ceramic powder, and the ceramic powder is agitated and mixed with water or an organic solvent, an organic binder, a dispersant, an antifoaming agent, and so on in a ball mill to yield a ceramic slurry.

[0038] The ceramic slurry is vacuum-defoamed, and is then formed into 80 μm thick plain ceramic green sheets by the doctor blade method.

[0039] Internal conductive layer patterns 41 are printed on some of the plain ceramic green sheets with an electroconductive paste containing Ag and Pd in a weight ratio of 7:3 to prepare internal conductive layer ceramic green sheets 31. In this instance, the printing conditions are controlled so that the paste of the internal conductive layer pattern 41 is applied at a thickness of about 1.0 μm.

[0040] Also, crack-forming conductive layer patterns 42 are printed on other plain ceramic green sheets with an electroconductive paste containing Ag and Pd in a weight ratio of 7:3 to prepare crack-forming conductive layer ceramic green sheets 32. In this instance, the printing conditions are controlled so that the paste of the crack-forming conductive layer pattern 42 is applied at a thickness of about 2.0 μm. The thicknesses of the internal conductive layer pattern 41 and the crack-forming conductive layer pattern 42 refer to the metal thicknesses measured by fluorescent X-ray spectrometry.

[0041] The internal conductive layer patterns 41 and the crack-forming conductive layer patterns 42 are each in contact with at least one edge of the corresponding ceramic green sheet so that they can be connected to the subsequently

formed external electrodes.

[0042] The internal conductive layer ceramic green sheets 31, the crack-forming conductive layer ceramic green sheets 32, and plain ceramic green sheets 33 are stacked as shown in Fig. 3 to prepare a green stack. The internal conductive layer ceramic green sheets 31 are alternately stacked so that the internal conductive layer patterns 41 are led out alternately to the side ends in the lateral direction. Also, the internal conductive layer ceramic green sheets 31 and the crack-forming conductive layer green sheets 32 are alternately stacked. The plain ceramic green sheets 33 are disposed at both ends of the stack in the stacking direction.

[0043] The resulting green stack is heated to 400°C to debinder, and is then fired at 1100°C for 5 hours in anormal atmosphere to yield the stack 10. The resulting stack 10 measures 7 mm by 7 mm and 30 mm in height.

[0044] Then, an electroconductive paste containing Ag is patterned to form the external electrodes 21 and 22 shown in Fig. 1. Subsequently, Ag nets are bonded to the external electrodes 21 and 22 with an electroconductive adhesive to reinforce the external electrodes 21 and 22, and lead wires are bonded to the external electrodes 21 and 22 with solder, but the nets and wires are not shown in the figure. The side surfaces of the stack 10 are coated with an insulating resin to insulate the internal conductive layers 12 exposed at the side surfaces of the stack 10.

[0045] The external electrodes 21 and 22 are connected to a direct current source and polarized at an electric field intensity of 3 kV/mm in a thermostatic chamber of 80°C. Thus the monolithic piezoelectric element shown in Fig. 1 is completed.

[0046] Samples were prepared in the following procedure for measuring the interfacial strengths between the internal conductive layer and the ceramic layer and between the crack-forming conductive layer and the ceramic layer.

[0047] The same ceramic green sheets as used in the above-described monolithic piezoelectric element were prepared, and internal conductive layer patterns were printed at the same thickness in the same manner as above. Five ceramic green sheets with the internal conductive layer pattern were stacked, and 20 plain ceramic green sheets were pressure-bonded to the bottom and top of the stack. The entire stack was fired under the same condition as above. Then, the resulting sintered compact was cut into samples of 3 mm by 3 mm and 2.5 mm in height for measuring the interfacial strength between the internal conductive layer and the ceramic layer.

[0048] Samples for measuring the interfacial strength between the crack-forming conductive layer and the ceramic layer were also prepared in the same manner.

[0049] Each of the resulting samples was measured for the peel force between the internal conductive layer and the ceramic layer or between the crack-forming conductive layer and the ceramic layer when they were separated from each other using a tensile test apparatus, with a jig provided to the top and bottom surface of the sample. Table 1 shows the results, Weibull values m obtained by Weibull-plotting the measured values and average strength μ.

[Table 1]

	Weibull coefficient m	Average strength μ (MPa)
Internal conductive layer/ceramic layer	5.1	72.4
Crack-forming conductive layer/ceramic layer	4.3	37.6

It is found that the interfacial strength between the crack-forming conductive layer and the ceramic layer is reduced to less than the interfacial strength between the internal conductive layer and the ceramic layer by setting the thickness of the crack-forming conductive layer 13 at twice the thickness of the internal conductive layer 12.

[0050] In addition, samples of a comparative example were prepared in the same manner except that the crack-forming conductive layers are not provided (Comparative Example 1). The states of three monolithic piezoelectric elements of the present embodiment and three monolithic piezoelectric elements of Comparative Example 1 were observed through a microscope after polarization.

[0051] In the monolithic piezoelectric element of the present embodiment, 12.6 cracks were produced on average per element. Each crack occurred in the vicinity of the crack-forming conductive layer and was very small. There was not a crack extending to the piezoelectrically active region.

[0052] On the other hand, 4.3 cracks were produced on average per element in the monolithic piezoelectric elements of the comparative example, but about one half of the cracks extended to the piezoelectrically active region.

[0053] Five monolithic piezoelectric elements each of the present embodiment and the comparative example were subjected to a continuous driving test at a temperature of 30°C and a humidity of 60% by applying rectangular waves of 200 V in maximum voltage and 30 Hz in frequency.

[0054] All the five monolithic piezoelectric elements of the present embodiment were normally operated after being driven 10^9 times. The distortions before and after the driving test were compared, and the degradation in distortion was within 5% in all the samples. On the other hand, all the monolithic piezoelectric elements of the comparative example were mechanically damaged, and were not operational after being driven 10^5 times.

[0055] Samples including the crack-forming conductive layers at intervals varied by thinning out some of the crack-forming conductive layers were prepared. More specifically, each monolithic piezoelectric element was prepared such that crack-forming conductive layers are not provided at the interfaces between specific internal conductive layers and thus the interval between the crack-forming conductive layers was varied, while in the structure shown in Figs. 1 and 3, the ceramic layers 11 having the internal conductive layers 12 (internal conductor ceramic green sheets 31) and the ceramic layers 11 having the crack-forming conductive layers 13 (crack-forming conductive layer ceramic green sheets 32) are alternately disposed. In this instance, plain ceramic layers were disposed in regions from which the ceramic layers having the crack-forming conductive layers were thinned out so that the intervals between the internal conductive layers in the stacking direction were the same. In this example, the ceramic layers 11 having the crack-forming conductive layers 13 were arranged substantially equally in the stacking direction of the stack.

[0056] Thus, seven types of samples were prepared. Five samples each of the seven types and Comparative Example 1 of the monolithic piezoelectric element were subjected to the continuous driving test in the same manner as above.

[0057] The distortion per section, D/M, was calculated. The sections were defined by dividing the stack by the surfaces of stacked layers on which the crack-forming conductive layers were disposed, and the number of sections was designated by M.

[0058] When the number of surfaces on which the crack-forming conductive layers are disposed is N, M is expressed by equation (1). More specifically, when, for example, the crack-forming conductive layers are formed on two surfaces of the stacked layers, M = 3 holes. If there is no crack-forming conductive layer on the surfaces of stacked layers, M = 1 holes.

$$M = N + 1 \qquad (1)$$

[0059] The results of measurement for distortion per section, D/M, and continuous driving test are shown in Table 2. Table 2 also shows the dimension of the section in the stacking direction, L/M (L represents a dimension of the stack in the stacking direction) for reference. In Sample 7, the crack-forming conductive layers are disposed in all the regions between two adjacent internal conductive layers.

[Table 2]

Sample No.	Number of crack-forming conductive layers	Dimension per section L/M (mm)	Distortion per section D/M (μm)	Number of samples that were able to be driven at the point of driving times					
				10^4	10^5	10^6	10^7	10^8	10^9
1	2	10	15	5	5	5	3	1	0
2	5	5.0	7.5	5	5	5	5	5	4
3	7	3.75	5.6	5	5	5	5	5	5
4	9	3.0	4.5	5	5	5	5	5	5
5	11	2.5	3.8	5	5	5	5	5	5
6	14	2.0	3.0	5	5	5	5	5	5
7	273	0.1	0.16	5	5	5	5	5	5
Comparative Example 1	0	30	45	4	0	0	0	0	0

[0060] As shown in Table 1, one of the monolithic piezoelectric elements of the comparative example did not work at the point of 10^4 times, and all of them did not work at the point of 10^5 times.

[0061] On the other hand, the monolithic piezoelectric elements of Sample Nos. 1 to 7 according to the present invention exhibited enhanced durability against continuous driving in contrast to Comparative Example 1. In Sample Nos. 3 to 7, particularly, all the elements were able to be driven even at the point of 10^9 times. This suggests that it is preferable that the crack-forming conductive layers are disposed so as to set the distortion between the crack-forming conductive layers to less than 7.5 μm.

[0062] While the crack forming conductive layer patterns are formed into rectangular shape in the present embodiment,

the shape of the crack-forming conductive layer patterns is not limited to rectangle. For example, the shape may be semicircular, as shown in Fig. 4.

Embodiment 2

[0063] A monolithic piezoelectric element according to a second embodiment of the present invention will now be described. Descriptions of elements that are the same as or corresponding to those of the first embodiment will be omitted as needed. Fig. 5 is a sectional view of a monolithic piezoelectric element according to a second embodiment.

[0064] The monolithic piezoelectric element includes a stack 10 and external electrodes 21 and 22. The stack 10 includes integrally formed ceramic layers 11, internal conductive layers 12 and crack-forming conductive layers 13. Although this structure is different from that of the first embodiment in that the crack-forming conductive layer 13 and the internal conductive layer 12 are disposed on the same surfaces of the stacked layers, and the other parts are the same as in the first embodiment.

[0065] The process for manufacturing the monolithic piezoelectric element will be described below with reference to Fig. 6. First, predetermined weights of metal oxides, such as titanium oxide, zirconium oxide, and lead oxide, are weighed out, and the mixture is calcined to yield a piezoelectric PZT ceramicss. The piezoelectric PZT ceramics is pulverized into piezoelectric ceramic powder, and the ceramic powder is agitated and mixed with water or an organic solvent, an organic binder, a dispersant, an antifoaming agent, and so on in a ball mill to yield a ceramic slurry.

[0066] The ceramic slurry is vacuum-defoamed, and is then formed into plain ceramic green sheets with a thickness of about 160 μm by the doctor blade method.

[0067] Now, an electroconductive paste for internal conductive layers is prepared by mixing Ag powder, Pd powder, the same piezoelectric ceramic powder as used in the formation of the ceramic green sheets, and an organic vehicle. Also an electroconductive paste for the crack-forming conductive layer is prepared by mixing Ag powder, Pd powder, and an organic vehicle. The ratio of the Ag content to the Pd content is Ag:Pd = 7:3 in both pastes.

[0068] Internal conductive layer patterns 41 are screen-printed on some of the plain ceramic green sheets with the electroconductive paste for internal conductive layers. Crack-forming conductive layer patterns 42 are further screen-printed with the electroconductive paste for the crack-forming conductive layers. Thus, conductor ceramic green sheets 34 are prepared. The internal conductive layer pattern 41 and the crack-forming conductive layer pattern 42 are led out to one and the other of the opposing side ends of the conductor ceramic green sheet 34, respectively.

[0069] The printing conditions are controlled so that the internal conductive layer pattern has a thickness of 1.4 μm and the crack-forming conductive layer pattern 42 has a thickness of 2.0 μm. The thicknesses of the patterns refer to the metal thicknesses measured by fluorescent X-ray spectrometry.

[0070] The conductor ceramic green sheets 34 and plain ceramic green sheets 33 are stacked as shown in Fig. 5 to prepare a green stack. The green stack is heated to 400°C to debinder, and is then fired at 1100°C for 5 hours in a normal atmosphere to yield the stack 10 shown in Fig. 4. The resulting stack 10 measures 7 mm x 7 mm and 30 mm in height.

[0071] Then, an electroconductive paste containing Ag is patterned on surfaces of the stack 10 to form the external electrodes 21 and 22. Subsequently, Ag nets are bonded to the external electrodes 21 and 22 with an electroconductive adhesive to reinforce the external electrodes 21 and 22, and lead wires are bonded to the external electrodes 21 and 22 with solder, but the nets and wires are not shown in the figure. The side surfaces of the stack 10 are coated with an insulating resin to insulate the internal conductive layers exposed at the side surfaces of the stack 10.

[0072] The external electrodes 21 and 22 are connected to a direct current source and polarized at an electric field intensity of 3 kV/mm in a thermostatic chamber of 80°C. Thus the monolithic piezoelectric element shown in Fig. 5 is completed.

[0073] Samples were prepared in the following procedure for measuring the interfacial strengths between the internal conductive layer and the ceramic layer and between the crack-forming conductive layer and the ceramic layer.

[0074] The same ceramic green sheets as used in the monolithic piezoelectric element were prepared, and internal conductive layer patterns were printed using the same internal conductive layer conductive paste as above. Five ceramic green sheets with the internal conductive layer pattern were stacked, and 10 plain ceramic green sheets were press-bonded to the bottom and top of the stack. The entire stack was fired under the same conditions as above. Then, the resulting sintered compact was cut into samples of 3 mm by 3 mm and 2.5 mm in height for measuring the interfacial strength between the internal conductive layer and the ceramic layer.

[0075] Test pieces for measuring the interfacial strength between the crack-forming conductive layer and the ceramic layer were also prepared in the same manner using the same crack-forming conductive layer electroconductive paste as above.

[0076] Each of the resulting test pieces was measured for the peel force between the internal conductive layer and the ceramic layer or between the crack-forming conductive layer and the ceramic layer when they were separated from each other using a tensile test apparatus, with a jig provided to the top and bottom surface of the test piece. Table 3

shows the results, Weibull value m obtained by Weibull-plotting the measured values and average strength μ.

[Table 3]

	Weibull coefficient m	Average strength μ (MPa)
Internal conductive layer/ceramic layer	4.8	74.2
Crack-forming conductive layer/ceramic layer	4.3	37.6

[0077] It is found that the interfacial strength between the internal conductive layer and the ceramic layer is increased by adding to the internal conductive layer a ceramics having the same composition as the ceramic contained in the ceramic layer, in comparison with the interfacial strength between the crack-forming conductive layer, which does not contain the ceramics, and the ceramic layer.

[0078] In addition, monolithic piezoelectric elements of a comparative example were prepared in which only the internal conductive layer patterns were formed on the conductor ceramic green sheets, but the crack-forming conductive layer patterns are not formed (Comparative Example 2).

[0079] The monolithic piezoelectric elements of the present embodiment and the monolithic piezoelectric elements of the comparative example were observed through a microscope after polarization. Four cracks extending to the piezoelectrically active region were observed in the monolithic piezoelectric elements of Comparative Example 2. As for the monolithic piezoelectric elements of the present embodiment, 14 cracks, more than in comparative example 2, were observed, but each crack was formed in the piezoelectrically inactive region around the crack-forming conductive layer. There was not a crack extending to the piezoelectrically active region.

[Table 4]

	Number of samples that were able to be driven at the point of driving times					
	10^4	10^5	10^6	10^7	10^8	10^9
Example 2	5	5	5	5	5	5
Comparative Example 2	4	0	0	0	0	0

[0080] As shown in Fig. 4, one of the monolithic piezoelectric elements of Comparative Example 2 did not work properly at the point of 10^4 times due to mechanical damage, and all the samples did not work properly after being driven 10^5 times. On the other hand, all the samples of the monolithic piezoelectric element of the present embodiment worked properly even after being driven 10^9 times.

[0081] While the present embodiment forms rectangular crack-forming conductive layer patterns, the shape of the crack-forming conductive layer patterns is not limited to rectangle. For example, it may be semicircular, as shown in Fig. 7.

[0082] The above-disclosed embodiments 1 and 2 are simply examples of the invention, and the invention is not limited to the disclosed embodiments. For example, the crack-forming conductive layer may be formed in any shape anywhere as long as it can form a tiny crack in the piezoelectrically inactive region without extending to the piezoelectrically active region. The technique for reducing the interfacial strength between the crack-forming conductive layer and the ceramic layer to less than the interfacial strength between the internal conductive layer and the ceramic layer is not limited to the above method, and any technique may be applied. In addition, other modifications may be made without departing from the spirit and scope of the invention.

Claims

1. A monolithic piezoelectric element comprising: a stack including piezoelectric ceramic layers and internal conductive layers that are integrally formed; and external electrodes disposed on a surface of the stack,
wherein the stack further includes a crack-forming conductive layer inside so as to form a crack in the stack.

2. The monolithic piezoelectric element according to Claim 1, wherein the interfacial strength between the crack-forming conductive layer and the ceramic layer is lower than an interfacial strength between the internal conductive layer and the ceramic layer.

3. The monolithic piezoelectric element according to Claim 2, wherein an internal conductive layers contains a ceramic having the same composition system as the ceramic contained in the ceramic layers, and

wherein the crack-forming conductive layer does not contain the ceramic having the same composition as the ceramic of the ceramic layer, or contains the ceramic in a lower content than the internal conductive layer.

4. The monolithic piezoelectric element according to Claim 2 or 3, wherein the crack-forming conductive layer has a larger thickness than the internal conductive layer.

5. The monolithic piezoelectric element according to any one of Claims 1 to 4, wherein the crack-forming conductive layer is disposed along a surface of the layers of the stack, and lie on the same surfaces as the internal conductive layers.

6. The monolithic piezoelectric element according to any one of Claims 1 to 4, wherein the crack-forming conductive layer is disposed along a surface of the layers of the stack, and lie on surfaces on which the internal conductive layers are not formed.

7. The monolithic piezoelectric element according to any one of Claims 1 to 6, wherein the crack-forming conductive layer is disposed in a region where the internal conductive layers do not overlap in a direction in which layers are stacked.

8. The monolithic piezoelectric element according to any one of Claims 1 to 7, wherein when sections are defined by dividing the stack by the surfaces of layers on which the crack-forming conductive layer is disposed, the number of sections is M, and the distortion in a direction in which layers are stacked is D (μm), the distortion per section D/M is 7.5 μm or less.

FIG. 1

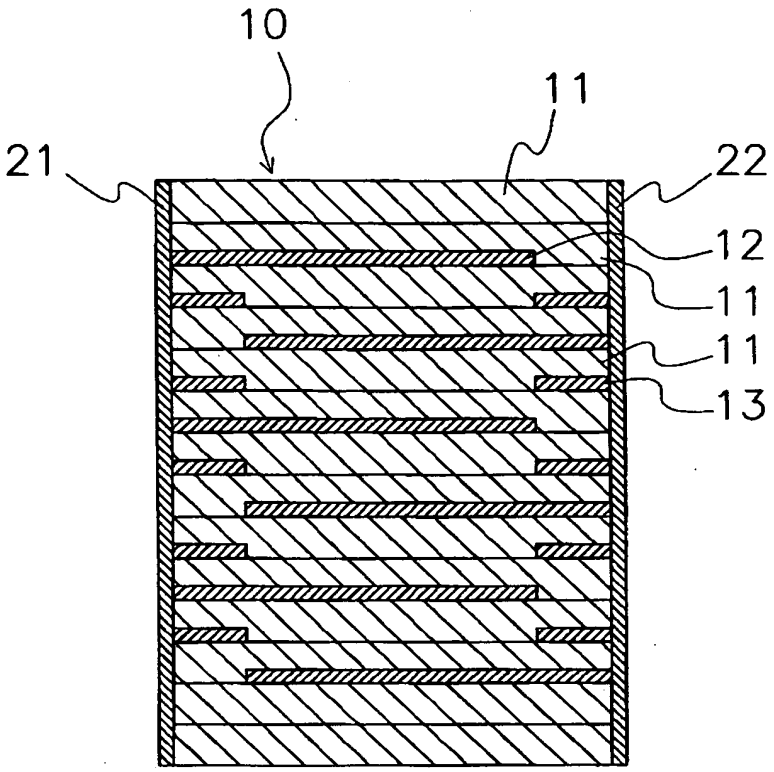


FIG. 2

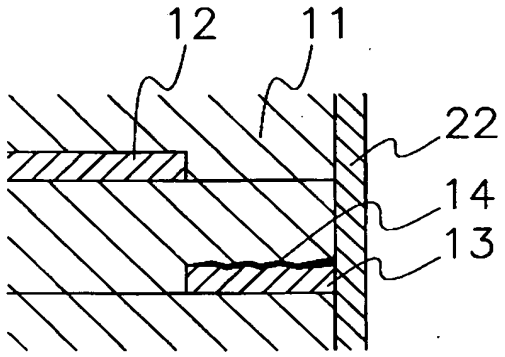


FIG. 3

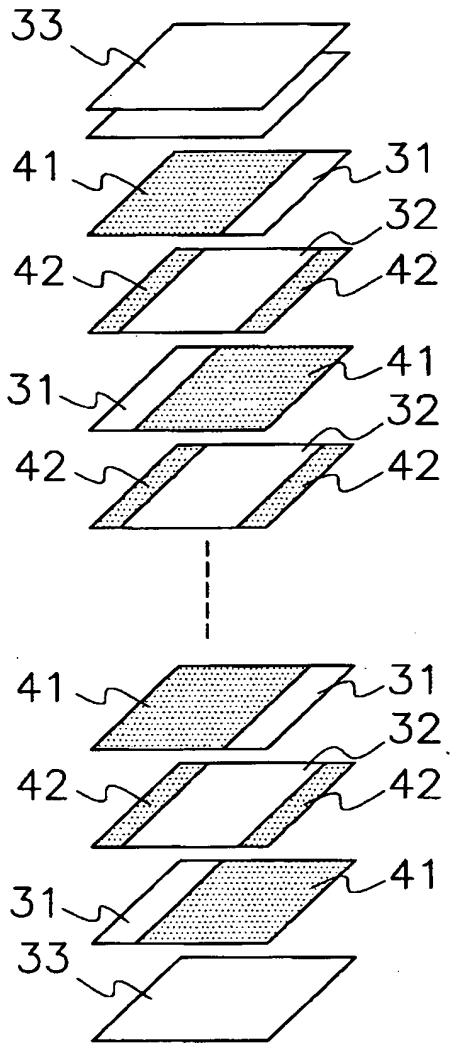


FIG. 4

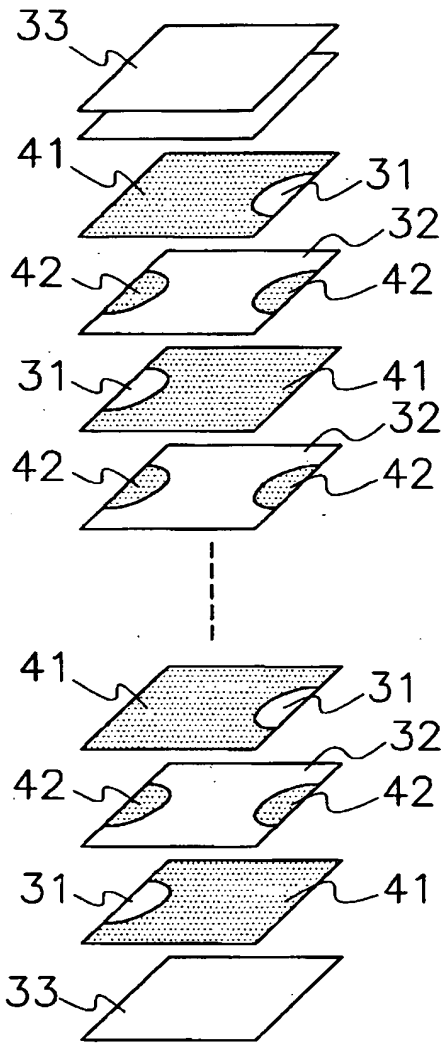


FIG. 5

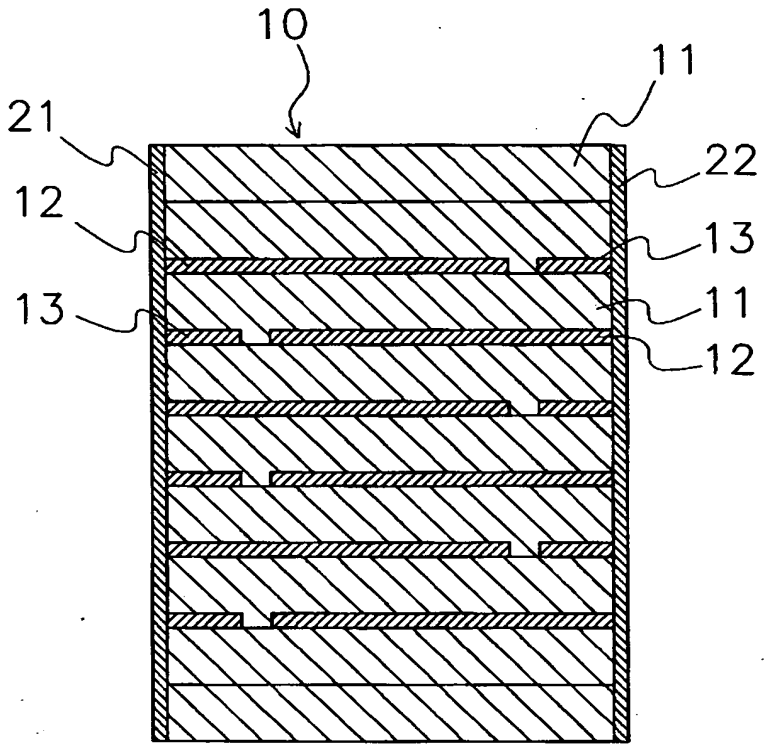


FIG. 6

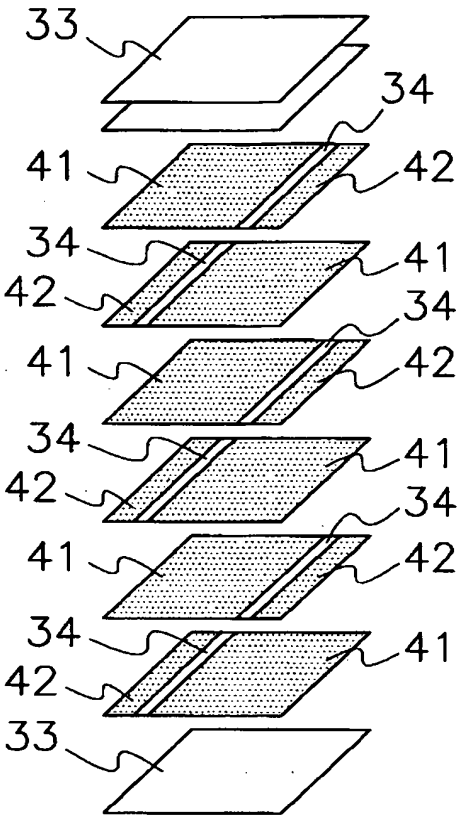
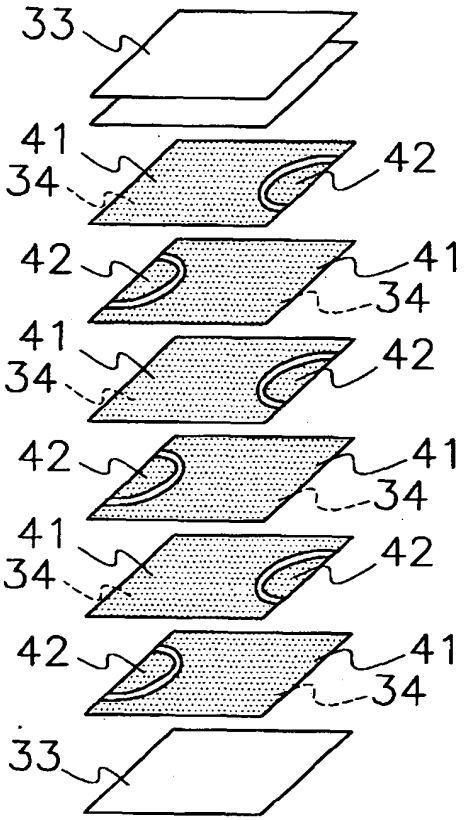


FIG. 7



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2005/023651

A. CLASSIFICATION OF SUBJECT MATTER
H01L41/083(2006.01), ***H01L41/187***(2006.01), ***H01L41/22***(2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L41/083(2006.01), ***H01L41/187***(2006.01), ***H01L41/22***(2006.01)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2006
Kokai Jitsuyo Shinan Koho 1971-2006 Toroku Jitsuyo Shinan Koho 1994-2006

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 2001-24247 A (Matsushita Electric Industrial Co., Ltd.), 26 January, 2001 (26.01.01), Par. No. [0032]; Fig. 4 (Family: none)	1-8
A	JP 61-124183 A (Nippon Soken, Inc.), 11 June, 1986 (11.06.86), Page 3, lower right column, lines 13 to 20; Fig. 1 (Family: none)	1-8
A	JP 6-204581 A (Tokin Corp.), 22 July, 1994 (22.07.94), Par. No. [0002]; Fig. 5 (Family: none)	1-8

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
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"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
14 February, 2006 (14.02.06)	28 February, 2006 (28.02.06)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2005/023651

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	JP 4-299588 A (NEC Corp.), 22 October, 1992 (22.10.92), Par. Nos. [0004] to [0005]; Fig. 2 & US 5196757 A Page 1, right column, line 43 to left column, line 8; Fig. 3	2-8

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REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 6005794 B **[0007]**

PUB-NO: EP001850403A1

DOCUMENT-IDENTIFIER: EP 1850403 A1

TITLE: MULTILAYER PIEZOELECTRIC DEVICE

PUBN-DATE: October 31, 2007

INVENTOR-INFORMATION:

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APPL-NO: EP05820084

APPL-DATE: December 22, 2005

PRIORITY-DATA: JP2005038232A (February 15, 2005)

INT-CL (IPC): H01L041/083

EUR-CL (EPC): H01L041/083

ABSTRACT:

CHG DATE=20071102 STATUS=O>To provide a monolithic piezoelectric element that can be

easily manufactured while the stack is prevented from being mechanically broken by stress. The monolithic piezoelectric element includes a stack 10, and the stack 10 includes a crack-forming conductive layer 13 for forming a small crack therein. The small crack alleviates stress, thereby preventing the occurrence of such a large crack as extends to the piezoelectrically active region.